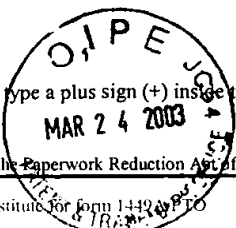


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				Application Number	09/535,015
				Filing Date	March 24, 2000
				First Named Inventor	Shunpei YAMAZAKI et al.
				Group Art Unit	2811
				Examiner Name	S. Crane
Sheet	1	of	1	Attorney Docket Number:	0756-2131

U.S. PATENT DOCUMENTS						
Examiner Initials [*]	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
SWC		4,759,610		Yanagisawa	07/26/1988	
SWC		5,535,471		Guldi	07/16/1996	
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FOREIGN PATENT DOCUMENTS							
Examiner Initials [*]	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials [*]	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
SWC		Wolf, <i>Silicon Processing for the VLSI ERA</i> , Volume 2: Process Integration, Page 274 (1990)	

Examiner Signature	CRANE	Date Considered	11/6/03
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